AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 1, 2, 4, 6, 9 and 10 without prejudice and amend claims 3, 5, 7, 8 and 11 as follows:

LISTING OF CLAIMS:

1. (Canceled).

2. (Canceled).

3. (Currently Amended) [[The]] A data processor ~~according to claim 1~~ which executes a program including a repeat block composed of plural instructions and processed repeatedly, said data processor comprising:

detecting means implemented by hardware, for detecting a break of repeat processing in said repeat block independently of an operation specified by an instruction being executed; and

instruction execution inhibit means responsive to the detection of said break of said repeat processing by said detecting means to inhibit execution of remaining instructions in said repeat block, wherein said instruction execution inhibit means is instruction processing sequence switching means for switching said instruction processing sequence to ~~the~~ a next instruction of said repeat block at an instruction fetch stage upon detection of said break of said repeat processing by said detecting means.

4. (Canceled).

5. (Currently Amended) [[The]] A data processor which executes a program including a repeat block composed of plural instructions and processed repeatedly, said data processor comprising:

detecting means implemented by hardware, for detecting a break of repeat processing in said repeat block independently of an operation specified by an instruction being executed; and

instruction execution inhibit means responsive to the detection of said break of said repeat processing by said detecting means to inhibit execution of remaining instructions in said repeat block ~~according to claim 4~~, wherein said instruction execution inhibit means is instruction processing sequence switching means for switching said instruction processing sequence to a next instruction of said repeat block at an instruction execution stage upon detection of said break of said repeat processing by said detecting means, and

wherein said instruction processing sequence switching means is means for performing jump processing to the next instruction of said repeat block during execution of a last instruction that is executed last in said repeat processing of said repeat block.

6. (Canceled).

7. (Currently Amended) [[The]] A data processor ~~according to claim 1~~ which executes a program including a repeat block composed of plural instructions and processed repeatedly, said data processor comprising:

detecting means implemented by hardware, for detecting a break of repeat processing in said repeat block independently of an operation specified by an instruction being executed; and

instruction execution inhibit means responsive to the detection of said break of said repeat processing by said detecting means to inhibit execution of remaining instructions in said repeat block, wherein said detecting means is means for deciding whether said repeat processing breaks, based on an address of an instruction that is executed during said repeat processing of said repeat block.

8. (Currently Amended) The data processor according to claim 7, wherein said detecting means has count means for counting ~~the~~ a number of repetitions of processing of said repeat block, and comparison means for comparing the address of the instruction to be currently processed in said repeat block with the address of ~~the~~ a last instruction to be executed last in said repeat processing of said repeat block, and wherein upon being informed from said comparison means of the coincidence of address between said instruction to be currently processed and said last instruction when the count number of said count means has reached a predetermined value, said detecting means decides that said repeat processing breaks.

9. (Canceled)

10. (Canceled).

11. (Currently Amended) [[The]] A data processor which executes a program including a repeat block composed of plural instructions and processed repeatedly, said data processor comprising:

detecting means implemented by hardware, for detecting a break of repeat processing in said repeat block independently of an operation specified by an instruction being executed; and

instruction execution inhibit means responsive to the detection of said break of said repeat processing by said detecting means to inhibit execution of remaining instructions in said repeat block ~~according to claim 9~~,

wherein said detecting means is means for deciding whether said repeat processing breaks, based on a number of instructions to be executed during repeat processing of said repeat block, and

wherein said detecting means has first count means for counting ~~the~~ a number of repetitions of processing of said repeat block and second count means for counting the number of instructions executed during each repeat processing of said repeat block, and said detecting means decides that said repeat processing breaks when ~~the~~ a count number of said first count means reaches a first predetermined value and the count number of said second count means reaches a second predetermined value in ~~the~~ a last repeat processing of said repeat block.